Deviationsheet

		JDI proposal		
If not mentioned, data is valid for 25°C, 60%rH		date 10.04.2013		
General characteristics		**JDI 12.3in 1920x720 Standard**		
Display technology		a-Si TFT, wide viewing angle technology		
Display Mode		Transmissive		
Format		Landscape (for portrait usage polarizer needs to be rotated)		
Screen size (Diagonal)		12.3in		
Display resolution		1920 x RGB x 720		
Active area size	(W x H) mm²	292.608 x 109.728		
Pixel size	(W x H) mm²	0.1524 mm		
Dot configuration		RGB vertical stripe		
Aspect Ratio		8:3		
Grey scale inversion direction		none		
Luminance perpendicular (Center, +25°C)		760Cd/m² min		
Contrast perpendicular (Center, +25°C)		1000:1 min		
Colour Depth		24-Bit		
Polarizer surface treatment	standard	AG (with retarder)		
Display surface reflection		4% typ for reference		
Operating Temperature (glass surface)		-30°C to +85°C		
Operating Temperature w/ limited performance		-40°C to -30°C: no damage, no malfunction		
Storage Temperature (ambient)		-40°C to +90°C		
Options	Photo sensor for B/L	n.a.		
	B/L Temp. Sensor / NTC	Yes		
	LCF	No		
	Coding resistor	No		
	Corner Cut	No		
	Display Heater	No		
	Heat Sink	No		
	Laminated cover glass	No		
	Touch Panel (Yes/No, Type)	No		
General Concept				
System to be delivered		TFT panel incl. Backlight		
Display PCB		excluded		
Timing Controller		excluded		
Integrated RAM		excluded		
Gamma voltage converter		excluded		
VCOM generator		excluded		
DC/DC converter		excluded		
Backlight driver		external		
Optical characteristics				
Area of Validity		All values have to be fulfilled with Touchpanel or LCF, if required:		
		Warm-Up Time before measurement: 30 min; Ambient Temp. (if not specified): +25°C		
		Backlight (if not specified): 100% PWM		
		All values will be measured perpendicular if there is no viewing angle (area) specified.		
		Reference for Color calculation and reflective measurements: D65 Standard Illuminant (ISO 10526:1999/CIE S005/E-1998), 2° Standard Observer (if not specifed)		
Polarized Sunglasses Readability		guaranteed		
Frame Rate		60Hz		
Luminance life time	@25°C	LED: Tamb 25degC (Tj<90degC), 80mA 20,000hrs to 50%		
Luminance life time	@85°C	-		
Contrast over viewing angle	L/R >100:1 min	80°/80° (min)		
	U/D >100:1 min	80°/80° (min)		
Response time (grey-to-grey)	Ta = +25°C	max(TG2G)≤ 30ms		
	Ta = -20°C	max(TG2G)≤ 250ms		
	Ta = -30°C	max(TG2G)≤ 700ms		
Chromaticity (x,y)		**x**	**y**	**tol. (±)**
Chromaticity (x,y)	White	0.313	0.329	0.035
	Red	0.620	0.308	0.035
	Green	0.299	0.606	0.035
	Blue	0.145	0.081	0.035
Colour Gamut NTSC (x/y)		78% typ		
Luminance homogenity White VESA 9point		75% min		

Gamma		2.2 +/-0.3 (VESA16, perpendicular, +25°C)
Electrical characteristics		
Electrical data interface	option	mini LVDS (tentative IF spec attached)
	option	Dual RSDS
Absolute maximum ratings	Data signal voltage	tbd
	Power supply	tbd
Data signal voltage	High (V)	tbd
	Low (V)	tbd
Power supply	VDD1 (V)	tbd
	IDD1 (mA)	tbd
Power supply	VDD2 (V)	tbd
	IDD2 (mA)	tbd
Power supply	VGH (V)	tbd
	VGL (V)	tbd
	VCOM (V)	tbd
Power consumption w/o backlight unit		tbd
Display Driving Technology		Dot inversion
Electro-mechanical I/F		ZIF
Backlight		
LED technology		white LED
Backlight layout	Number of LEDs per chain	8
	Number of LED chains	6
	Chain stucture	≥ 2 chains, combstructure wired
	LED type & # of ranks	NSSW157B
	LED brightness rank	2 ranks
	LED colour rank	3 ranks
	LED voltage	typ 3.0V/LED
	LED current	(86mA)
Power consumption LEDs		typ 10.8W
Mechanical Features		
Outline dimension	mm³	312.0 x 128.6 x 10.0 (w/o boss and FPC)
Quality Standards		
Bright Dot Defects		0
Test condition bright dots		backlight 100%; black picture; 10% ND filter, dark environment
Weak Bright Dot Defects	Red	0 (when more than 1/2 size of sub-pixel is bright on sub-pixel, the symptom is judged as bright dot. Bright dots other than pixel defects are defined as minor defect).
	Green	
	Blue	
Test condition bright dots		backlight 100%; white, red, green or blue picture; 10% ND filter; dark environment
Dark Dot Defects	Red	4
	Green	4
	Blue	4
Maximum joined dots	Bright	0
	Dark	2
Distance between 2 defects		>10mm
Cluster Dark Dot Defects (3 or more joined dot def.)		0
Maximum Dot Defects		4
Minor Defects	Dot defect	JDI standard
Reliability Tests		
Reliability tests		JDI standard
Scratch Resistance/ Surface Hardness		3H
Comment / Remarks		
All items not mentioned above		tbd

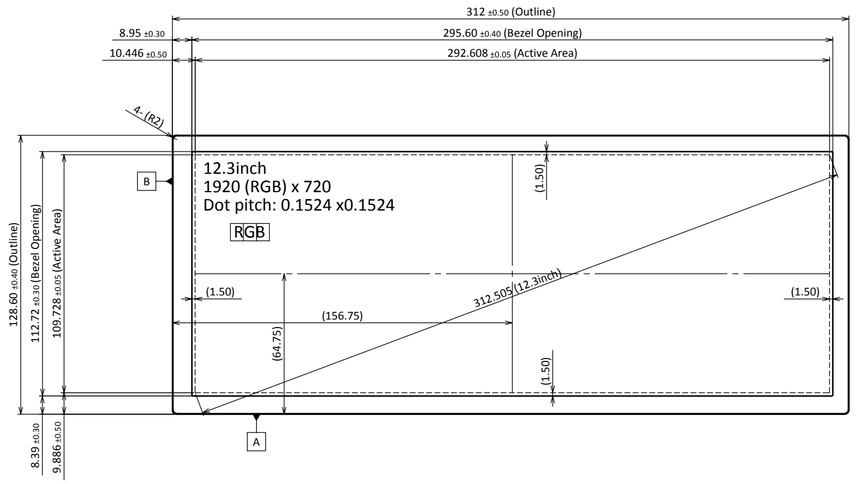
CONFIDENTIAL

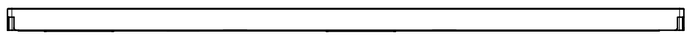
Japan Display Inc.

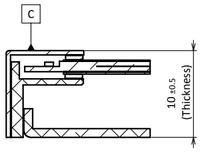
Definition of the DATUM A: Bottom side of the metal frame.
Definition of the DATUM B: Left side of the metal frame.
Definition of the DATUM C: Surface of the metal frame.

流用制限部品

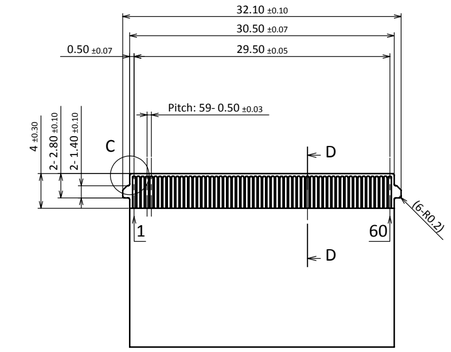
TENTATIVE



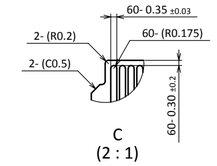




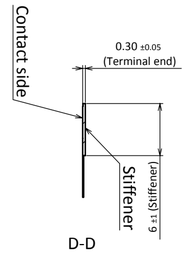
B-B



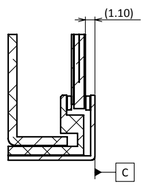
DATA FPC1 and 2 Detail
(Reverse side shown)
JDI's reccomendation connector
KYOCERA 6288 series



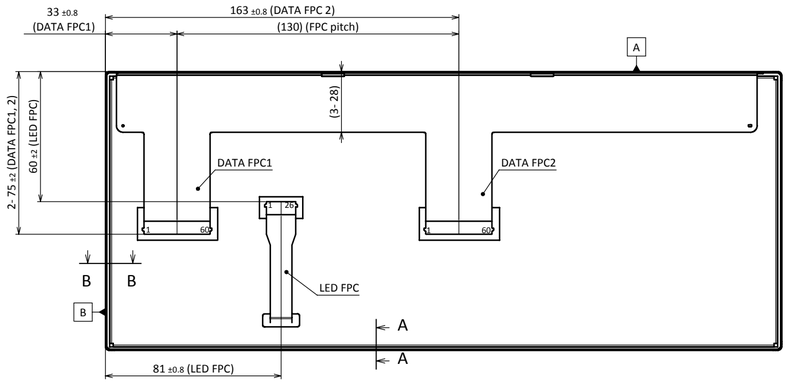
C
(2 : 1)

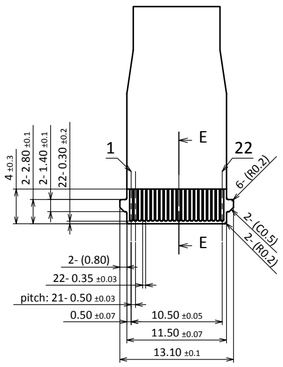


D-D

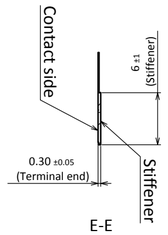


A-A

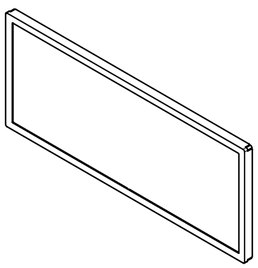




LED FPC Detail
(Reverse side shown)
JDI's recommendation connector
KYOCERA 6288 series



E-E



LED arrangement
12 LEDs x 4 strings
(8 LEDs x 6 strings applicable)
TTL: 48LEDs

Forward current: 82mA

Pin number	4 strings	6 strings
1	Cathode 1	Cathode 1
2	NC	NC
3	Anode 1	Anode 1
4	Anode 2	Anode 2
5	NC	NC
6	Cathode 2	Cathode 2
7	Cathode 3	Cathode 3
8	NC	NC
9	Anode 3	Anode 3
10	Anode 4	Anode 4
11	NC	NC
12	Cathode 4	Cathode 4
13	NC	Cathode 5
14	NC	NC
15	NC	Anode 5
16	NC	Anode 6
17	NC	NC
18	NC	Cathode 6
19	NC	NC
20	NTC	NTC
21	NTC	NTC
22	NC	NC

E CODE
M : *
P : *
D : *

HISTORY X COUNT | SUFFIX REPL | ECN-NO. DATE | REVISION | SIGN

DRAWN BY: I.Hashimoto
PLANNED BY
CHECKED BY
APPROVED BY
TENTATIVE
MODEL: *
PART NO.

UNIT: mm
ANGLE
SCALE: 1:2
TOLERANCE
USED NO
RANK
FAMILY
ORIGINAL MODEL: *
MATERIAL(COLOR)
FINISH(COLOR)

TITLE/DESCRIPTION
(E) 12.3inch 720HD TFT LCD outline drawing
(J)

PART NO.
SHEET 1/1

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A2
'12.4

ISSUED '12.11.07

F spec - D22

Tentative Interface Specification

LCD MODULE

Product number：12.2-HD Demo-sample

- 1920(RGB) x 720 dots
- mini-LVDS
- a-TFT color (24bit / pixel)

TENTATIVE

Valid for only demo-samples

	Date	Rev
Issued Date	Mar. 15, 2013	00

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

REVISION HISTORY

Product Number	Rev.	Revised item	Date
XXXXXX	00	Initial issue	Oct.,2, 2012

(C): Changed (A): Appended (D): Deleted (F): Filled in

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

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This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

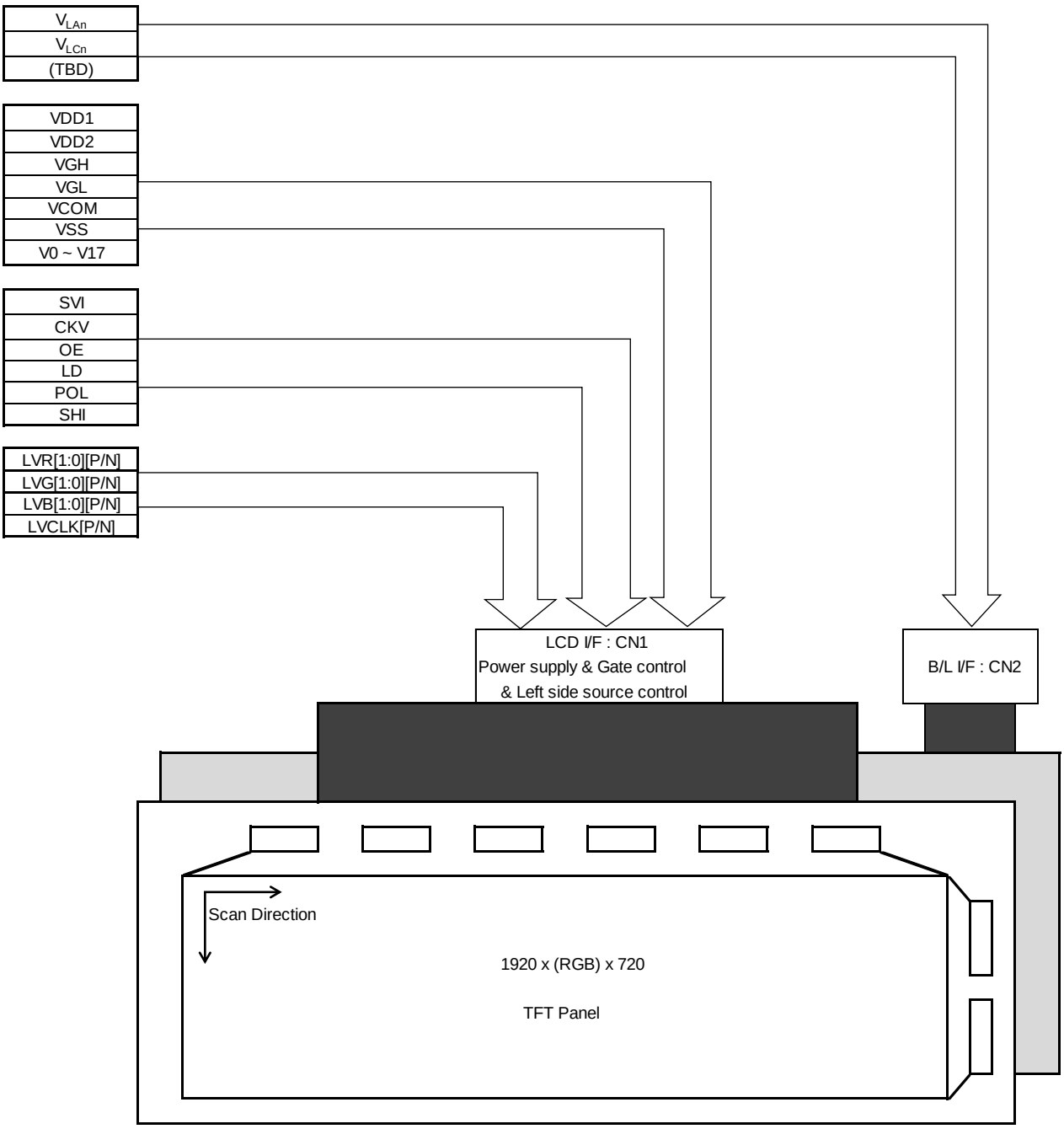
1. BASIC SPECIFICATIONS

This document gives the characteristics of the active matrix color TFT LCD which is designed for automotive use.

1.1 STRUCTURES

No.	FACTOR	SPECIFICATIONS	UNIT
1	LCD structure	a-TFT LCD	-
2	Number of dots	1920(W) x RGB x 720(H)	-
10	Operating Temperature (glass surface)	- 40 to +85	deg. C
11	Storage Temperature	- 40 to +90	deg. C

1.2 BLOCK DIAGRAM



This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

1.3 I/O TERMINALS

LCD I/F FPC

PIN	SYMBOL	FUNCTION	I/O	REMARKS
1	VSS	Ground	P	
2	SHI	Source starting pulse	I	
3	POL	Source polarity signal	I	
4	LD	Source latch pulse	I	
5	LVB1P	Mini LVDS input data (Blue, Pos.)	I	
6	LVB1N	Mini LVDS input data (Blue, Neg.)	I	
7	LVB0P	Mini LVDS input data (Blue, Pos.)	I	
8	LVB0N	Mini LVDS input data (Blue, Neg.)	I	
9	N.C.	No connect	-	
10	N.C.	No connect	-	
11	N.C.	No connect	-	
12	N.C.	No connect	-	
13	LVCLKP	Mini LVDS input clock (Pos.)	I	
14	LVCLKN	Mini LVDS input clock (Neg.)	I	
15	LVG1P	Mini LVDS input data (Green, Pos.)	I	
16	LVG1N	Mini LVDS input data (Green, Neg.)	I	
17	LVG0P	Mini LVDS input data (Green, Pos.)	I	
18	LVG0N	Mini LVDS input data (Green, Neg.)	I	
19	N.C.	No connect	-	
20	N.C.	No connect	-	
21	N.C.	No connect	-	
22	N.C.	No connect	-	
23	LVR1P	Mini LVDS input data (Red, Pos.)	I	
24	LVR1N	Mini LVDS input data (Red, Neg.)	I	
25	LVR0P	Mini LVDS input data (Red, Pos.)	I	
26	LVR0N	Mini LVDS input data (Red, Neg.)	I	
27	N.C.	No connect	-	
28	N.C.	No connect	-	
29	N.C.	No connect	-	
30	N.C.	No connect	-	
31	VSS	Ground	P	
32	V17	Gradation voltage	P	
33	V16	Gradation voltage	P	
34	V15	Gradation voltage	P	
35	V14	Gradation voltage	P	
36	V13	Gradation voltage	P	
37	V12	Gradation voltage	P	
38	V11	Gradation voltage	P	
39	V10	Gradation voltage	P	
40	V9	Gradation voltage	P	

P: power supply, I: input O: output

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

LCD I/F FPC

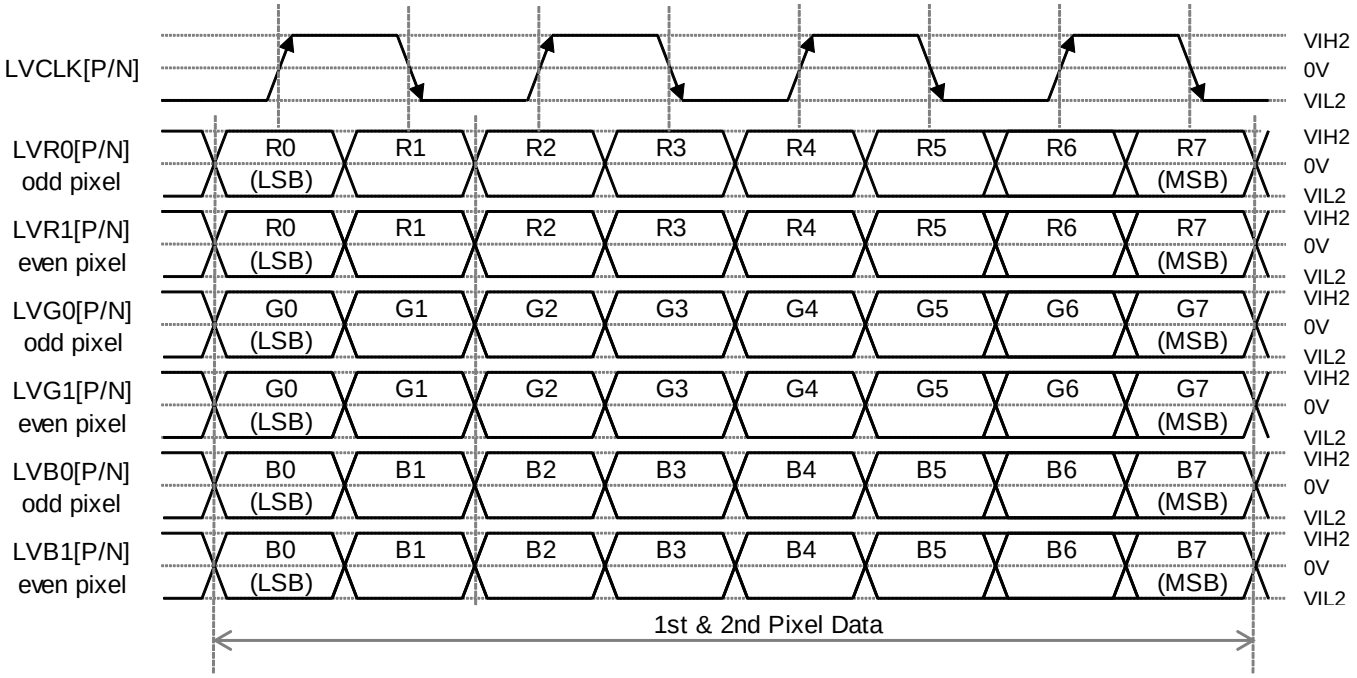
PIN	SYMBOL	FUNCTION	I/O	REMARKS
41	V8	Gradation voltage	P	
42	V7	Gradation voltage	P	
43	V6	Gradation voltage	P	
44	V5	Gradation voltage	P	
45	V4	Gradation voltage	P	
46	V3	Gradation voltage	P	
47	V2	Gradation voltage	P	
48	V1	Gradation voltage	P	
49	V0	Gradation voltage	P	
50	VDD2	Power supply for source	P	
51	VDD2	Power supply for source	P	
52	VSS	Ground	P	
53	VCOM	Common electrode power supply	P	
54	N.C.	No connect	-	
55	VGH	High level power supply for Gate	P	
56	N.C.	No connect	-	
57	VGL	Low level power supply for Gate	P	
58	N.C.	No connect	-	
59	SVI	Gate starting pulse	I	
60	OE	Enable output for Gate	I	
61	CKV	Shift clock for Gate	I	
62	N.C.	No connect	-	
63	VDD1	Power supply for logic	P	
64	VSS	Ground	P	

P: power supply, I: input O: output

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

2. FUNCTIONS

2.1 MINI-LVDS DATA MAPPING



This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

3. ABSOLUTE MAXIMUM RATINGS

Stress beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Extreme Ratings		Unit	Remarks
		Min.	Max.		
Power supplies voltage	VDD1	-0.3	4.0	V	Supply voltage for gate driver, source driver Condition : T_A = -40 up to + 85°C VSS = 0V
	VDD2	-0.3	18.0	V	
	VGH	-0.3	43.0	V	
	VGH-VGL	-0.3	43.0	V	
	VGL	-23.0	0.3	V	
Common Electrode Voltage	VCOM	-0.3	6.5	V	
Gradation sequence Voltage	V(0-8)	0.5 x VDD2 – 1.3	VDD2 + 0.3	V	
	V(9-17)	-0.3	0.5 x VDD2 + 1.3	V	
Input Signal Voltage (Video and Sync.)	LV(R/G/B)[1:0][P/N] LVCLK[P/N], SVI,CKV,OE, SHI,POL,LD	-0.3	VDD1 + 0.3	V	

3.2 ENVIROMENTAL ABSOLUTE MAXIMUM RATINGS

Parameter	Condition	Symbol	Rating		Unit	Remarks
			Min.	Max.		
Ambient temperature	Operation	TOP	-40	85	deg.C	No dew condition Note 1, 2
	Storage	TST	-40	90		

Note 1: Care should be taken so that the LCD module may not be subjected to the temperature beyond this specification.

Note2: Ambient temperature means the temperature at LCD surface. Module temperature is apt to increase while it's driving due to the heat of backlight etc. Design carefully not to exceed +85 deg.C at every point of LCD surface that should come to contact with any other equipment. In operation temperature range, only LCD operation is assured. Contrast, response time, or other LCD characteristics are specified in the condition of Ta = + 25 deg.C.

4. ELECTRICAL SPECIFICATION

4.1 DC CHARACTERISTICS OF POWER SUPPLY

GND = 0V

Parameter	Symbol	Condition	Standard Value			Unit	Remarks
			Min.	Typ.	Max.		
Power supply Voltage	VDD1		+3.0	+3.3	+3.6	V	
	VDD2		(+12.5)	(+13.0)	(+13.5)	V	
	VGH1		(+23.0)	(+24.0)	(+25.0)	V	
	VGH2		(+9.5)	(+10.0)	(+10.5)	V	gate driving waveform modulation
	VGL		(-5.5)	(-5.0)	(-4.5)	V	
Common electrode voltage	VCOM	Note 2	(+4.0)	-	(+6.0)	V	
Gradation voltage	V0 ~ V8		TBD	-	TBD	V	
	V9 ~ V17		TBD	-	TBD	V	
Power supply current	IDD1	Note 3	-	TBD	TBD	mA	
	IDD2		-	TBD	TBD	mA	
	IGH		-	TBD	TBD	mA	
	IGL		-	TBD	TBD	mA	
	ICOM		-	TBD	TBD	mA	
Permissive ripple	VDD1	Note 1	-	-	(+60)	mVpp	
	VDD2		-	-	(+40)	mVpp	
	VGH1		-	-	(+50)	mVpp	
	VGH2		-	-	(+40)	mVpp	
	VGL		-	-	(+80)	mVpp	
	VCOM		-	-	(+40)	mVpp	

Note 1:
When the ripple voltage frequency is synchronized with vertical or horizontal frequency, it might be visible even if it is less than specification.

Note 2:
VCOM adjustment step : less than 20mV.

Note 3
Measurement Condition: TBD

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

4.2 DC CHARACTERISTICS OF INPUT SIGNAL

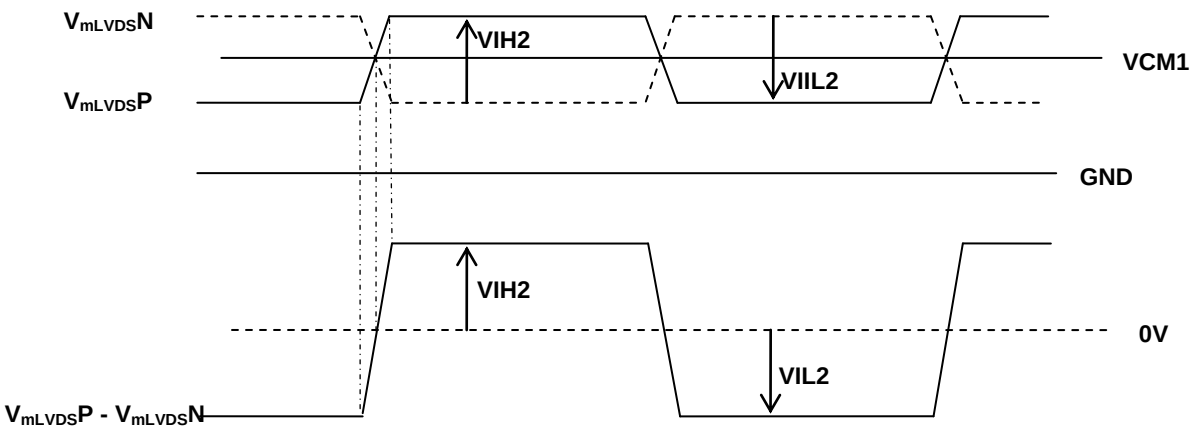
GND = 0V

Parameter	Symbol	Condition	Standard Value			Unit	Remarks
			Min.	Typ.	Max.		
Input signal voltage CMOS	VIH1		(0.8xVDD1)	-	VDD1	V	
	VIL1		VSS	-	(0.2xVDD1)	V	
Input signal voltage mini-LVDS	-		VSS	-	TBD	V	Input voltage range
	VIH2		TBD	+200	TBD	mV	Note 1
	VIL2		TBD	-200	TBD	mV	
Common voltage mini-LVDS	VCM1	(Vdiff1 = TBD)	(+0.5)	-	(+1.5)	V	

Note1:

Vdiff1 = $V_{mLVDS}P$- $V_{mLVDS}N$

VCM1= ($V_{mLVDS}P$+ $V_{mLVDS}N$)/2



This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

4.3 RELATIONSHIP BETWEEN GRADATION SEQUENCE AND VOLTAGE

Gradation Sequence	Positive Polarity	Negative Polarity
255d (FFh)	V0	V17
250d (FAh)	V1	V16
226d (E2h)	V2	V15
194d (C2h)	V3	V14
130d (82h)	V4	V13
64d (40h)	V5	V12
32d (20h)	V6	V11
4d (04h)	V7	V10
0d (00h)	V8	V9

Note

Gradation Sequence voltage should be kept on the following relation.

TBD ≥ V0 > V1 > V2 > V3 > V4 > V5 > V6 > V7 > V8 ≥ TBD

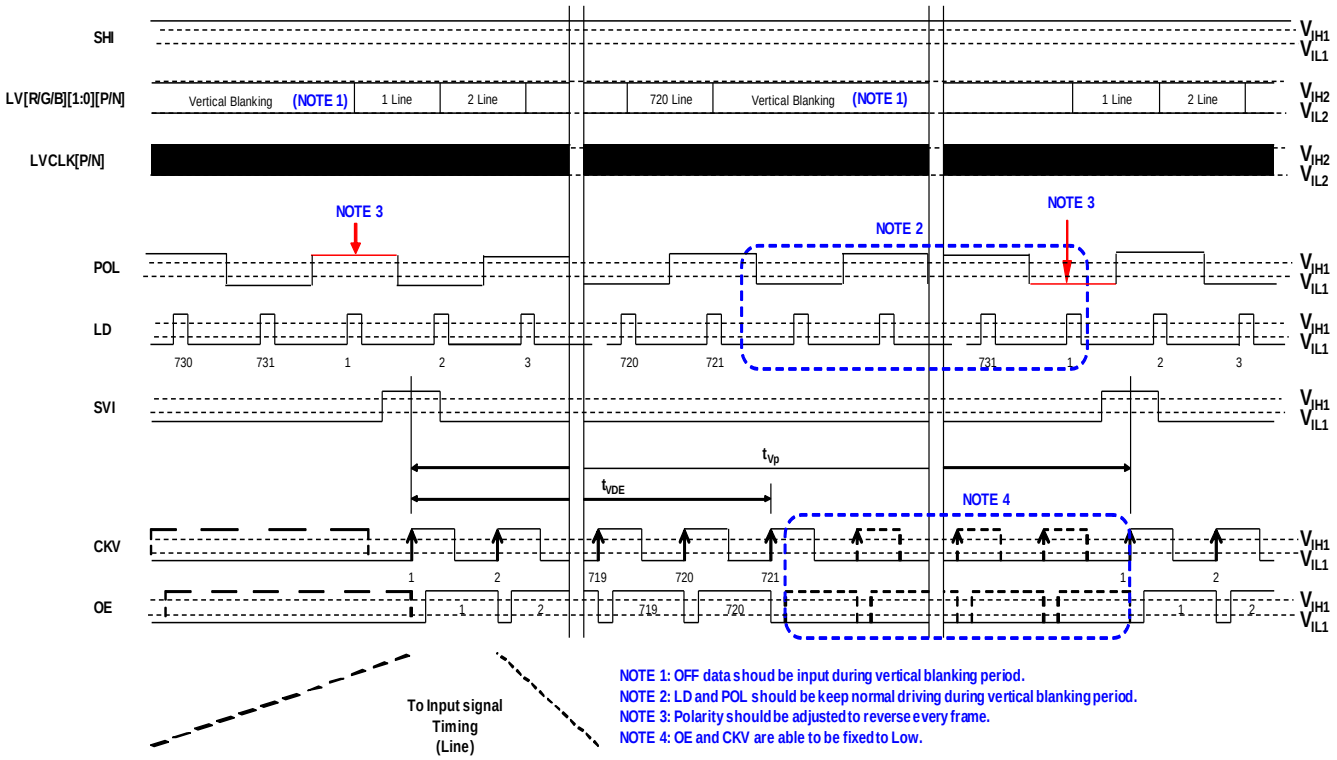
TBD ≥ V9 > V10 > V11 > V12 > V13 > V14 > V15 > V16 > V17 ≥ TBD

Gradation sequence voltages are needed a voltage follower circuit.

Symbol	STANDARD VALUE (REFERENCE)			Unit	Remarks
	γ= TBD	γ= 2.2	γ= TBD		
V0	TBD	TBD	TBD	V	
V1	TBD	TBD	TBD	V	
V2	TBD	TBD	TBD	V	
V3	TBD	TBD	TBD	V	
V4	TBD	TBD	TBD	V	
V5	TBD	TBD	TBD	V	
V6	TBD	TBD	TBD	V	
V7	TBD	TBD	TBD	V	
V8	TBD	TBD	TBD	V	
V9	TBD	TBD	TBD	V	
V10	TBD	TBD	TBD	V	
V11	TBD	TBD	TBD	V	
V12	TBD	TBD	TBD	V	
V13	TBD	TBD	TBD	V	
V14	TBD	TBD	TBD	V	
V15	TBD	TBD	TBD	V	
V16	TBD	TBD	TBD	V	
V17	TBD	TBD	TBD	V	

4.4 INTERFACE TIMING

4.4.1 Input Signal Timing (Frame)

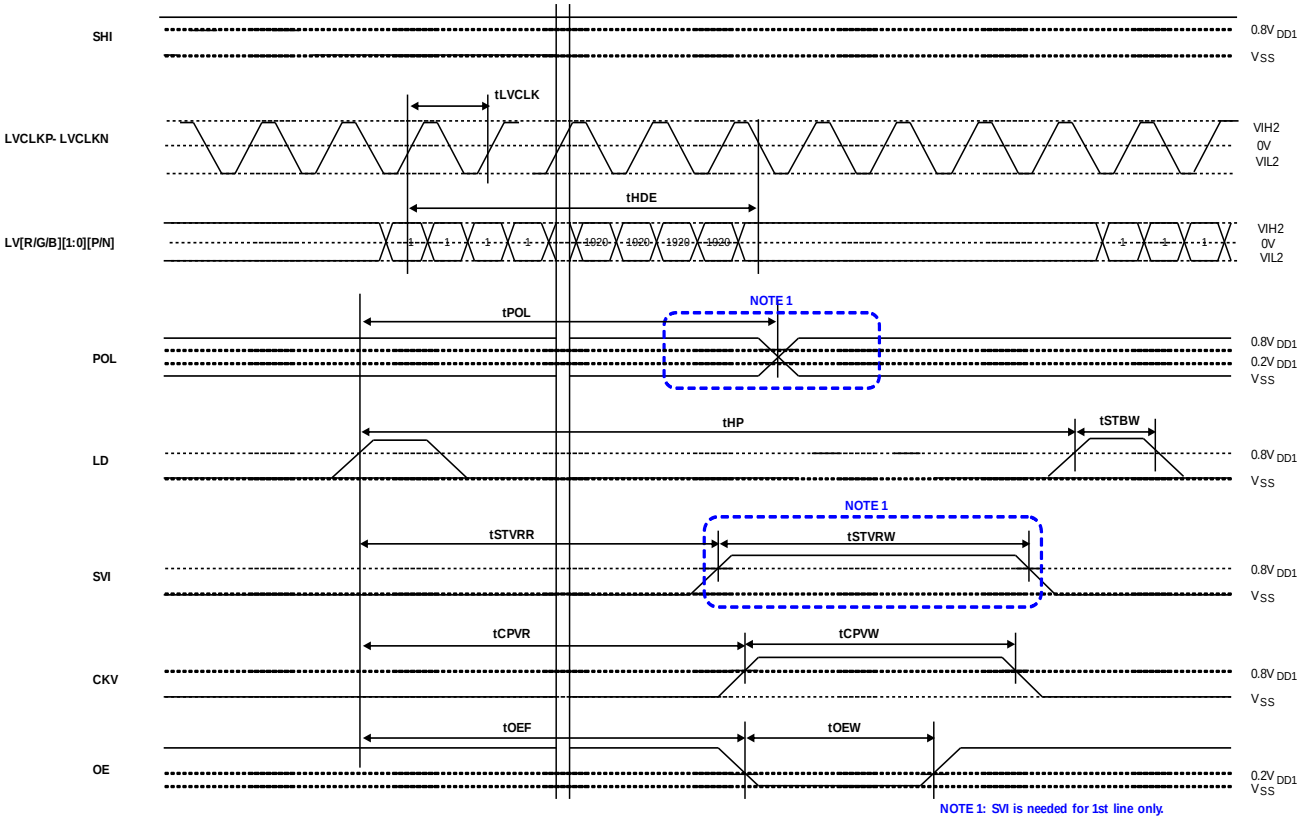


Note

VIH1, VIL1, VIH2 and VIL2 are in ranges of 4.2 DC CHARACTERISTICS OF INPUT SIGNAL.

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

4.4.2 Input Signal Timing (Line)

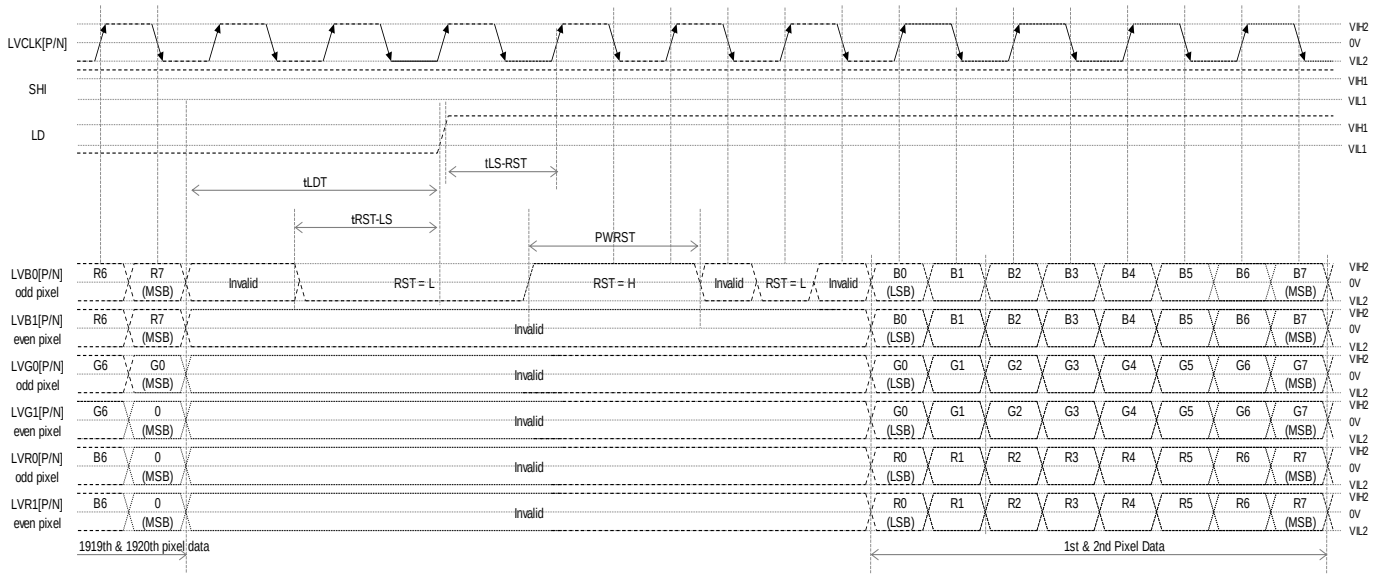


Note

VIH1, VIL1, VIH2 and VIL2 are in ranges of 4.2 DC CHARACTERISTICS OF INPUT SIGNAL.

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

4.4.3 Input Data Reset Timing



Note

VIH1, VIL1, VIH2 and VIL2 are in ranges of 4.2 DC CHARACTERISTICS OF INPUT SIGNAL.

4.4.4 Input Signal Timing Details

Parameter	Symbol	Condition	Standard Value			Unt	Remarks
			Min	Typ	Max		
LVCLK Freq.	1/tLVCLK		-	(200)	-	MHz	
Horizontal Period	tHP		-	(4560)	-	LVCLK	
Horizontal DE	tHDE		-	3840	-	LVCLK	
Vertical Period	tVP		-	(731)	-	Line	
Vertical DE	tVDE		-	720	-	Line	
RST high duration	PWRST		-	TBD	-	LVCLK	
LD Delay	tLDT		-	TBD	-	LVCLK	
RST to LD	tRST-LS		-	TBD	-	LVCLK	
LD to RST	tLS-RST		-	TBD	-	LVCLK	
LD Width	tSTBW		-	TBD	-	LVCLK	
LD to POL	tPOL		-	TBD	-	LVCLK	
LD-CKV	tCPVR		-	TBD	-	LVCLK	
CKV Width	tCPVW		-	TBD	-	LVCLK	
LD-OE	tOEF		-	TBD	-	LVCLK	
OE Width	tOEW		-	TBD	-	LVCLK	
LD-SVI	tSTVRR		-	TBD	-	LVCLK	
SVI Width	tSTVRW		-	TBD	-	LVCLK	

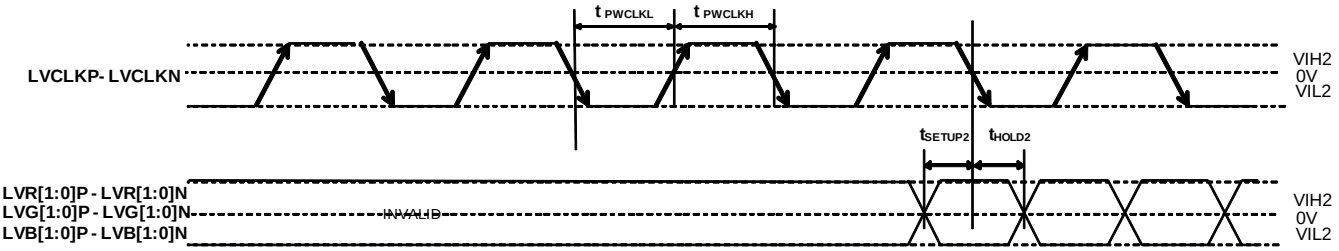
4.5 AC CHARACTERISTICS

Parameter	Symbol	Condition	Standard Value			Unt	Remarks
			Min	Typ	Max		
LVDATA- LVCLK Setup Time	tSETUP2	Note	TBD	-	-	ns	
LVCLK- LVDATA Hold Time	tHOLD2		TBD	-	-	ns	
LVCLK High Width	tPWCLKH		TBD	-	-	ns	
LVCLK Low Width	tPWCLKL		TBD	-	-	ns	

Note

The rise and fail times of all input signals (tr, tf) are equal or less than TBD ns. (mini-LVDS Signal)

tr and tr shall be 10 to 90% of their signal amplitude respectively.



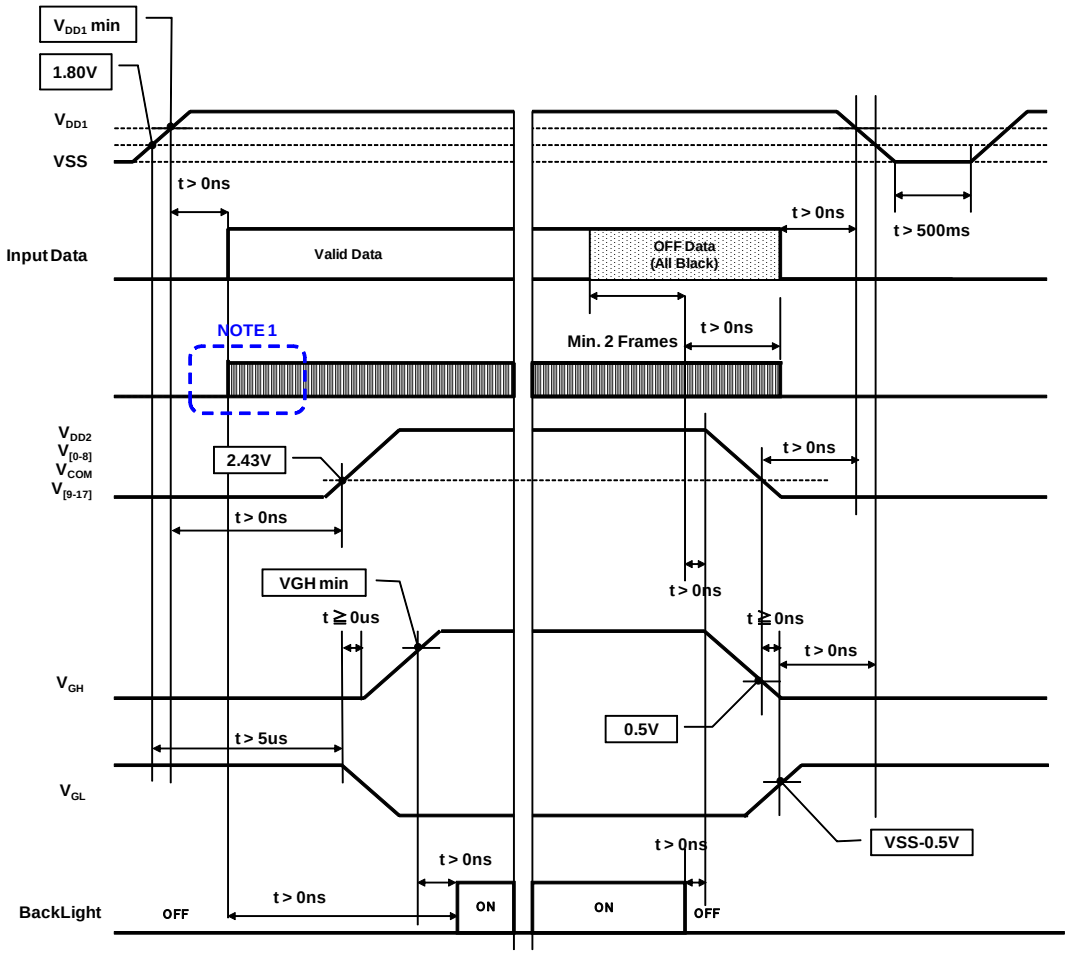
Note

VIH2 and VIL2 are in ranges of 4.2 DC CHARACTERISTICS OF INPUT SIGNAL.

4.6 GATE DRIVING WAVEFORM

TBD

4.7 RECOMMENDED SEQUENCE



NOTE

1) When power supply is OFF, logic input must be kept at either VSS level or high impedance

2) The rising speed of all power supplies should be less than 2V/100µs.
(All power supplies: V_{DD1}, V_{DD2}, V_{GH}, V_{GL}, V_{COM}, $V_{[0-17]}$)

3) Power up sequence: before turn on backlight, each power supply should reached a specification minimum voltage, and CKV and control signal should be inputted.
If it is not possible to satisfy, there is a potential unintended appears on the display.

4) After power supply VDD1, if it is neglected in the state where CKV is not inputted for a long time, the LCD module characteristic may be affected.

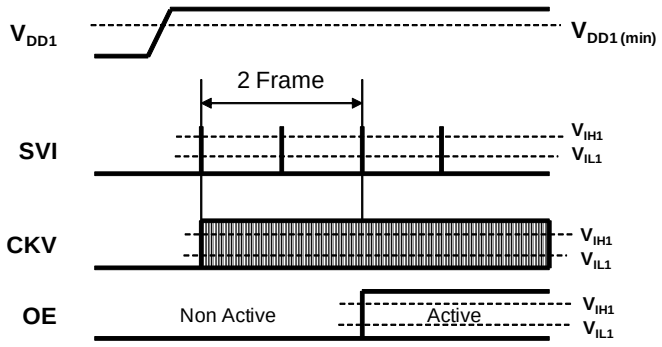
5) Min. 2 frames of OFF data are needed to be input, before power supply turns OFF.

6) Additionally, all voltages should be kept following level.
1. Less than 1.0V within 1 second.
2. Less than 30mV within 60 seconds.
(JDI recommends to inserting some discharge resistors in parallel with stable capacitor.
Especially, VGL, VCOM, VDD2 and V0~V17 should be inserted.)

This Interface Specification is preliminary. The official information is described in the LCD module specification after evaluation. The some value might vary for improvement the performance, quality and so on.

NOTE 1:

To reset the gate driver, input CKV by 2 frames with non-active OE.

Therefore abnormal display is appeared without the sequence.

VIH1 and VIL1 are in ranges of 4.2 DC CHARACTERISTICS OF INPUT SIGNAL.